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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,371	05/27/2005	Takuya Sugawara	101249.55458US	3837

23911 7590 03/31/2009

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EXAMINER	
LEE, CHEUNG	
ART UNIT	PAPER NUMBER
2812	
MAIL DATE	DELIVERY MODE
03/31/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/509,371	SUGAWARA ET AL.	
	Examiner	Art Unit	
	CHEUNG LEE	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,8,11-23,28-36,39-44,46,47,50,51 and 53-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8,11-23,29-36,41,42,44,46,47,51 and 53* is/are rejected.

7)☒ Claim(s) *28,39,40,43,50,54 and 55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Notice to Applicant

1. Applicants' Amendment and Response to the Office Action mailed on August 18, 2008 has been entered and made of record.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1, 16, 18, 20, 46 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyanagi (US Pub. 2002/0137239) in view of Buchanan et al. (US Pat. 6245616; hereinafter "Buchanan").

3. Referring to figures 1A-1C and related text, Koyanagi discloses [Re claim 1] a method for forming an underlying film, comprising: irradiating the surface of an insulating film 2 disposed on an electronic device substrate 1 with plasma based on a process gas comprising at least an oxygen atom-containing gas (page 4, paragraph 46), to thereby form an underlying film 3 at the interface between the insulating film and the electronic device substrate (page 4, paragraph 46, see fig. 1C), wherein the underlying film is an oxide film (page 4, paragraph 46), but Koyanagi fails to disclose expressly wherein the oxide film has a thickness of 6-12 Å.

Referring to figures 1-2B and related text, Buchanan discloses wherein after an oxynitride film 22 is formed, an oxide spacer layer 32 is formed between the oxynitride film and a silicon substrate 12 by a plasma CVD process (col. 6, lines 15-38; see fig. 2B). And the oxide spacer has a thickness between about 1 Å and about 40 Å (col. 4, lines 5-8).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a certain thickness of an underlying oxide, as taught by Buchanan,

because it would have been to obtain a desired oxide film without any leakage while keeping reduced size of a device.

4. Referring to figures 1A-1C and related text, Koyanagi discloses [Re claim 16] a method for forming an insulating film, comprising: forming a high-dielectric constant insulating film 2 on a substrate 1 (page 4, paragraph 45), generating plasma based on a process gas comprising at least an oxygen atom-containing gas on the high-dielectric constant insulating film (page 4, paragraph 46), and irradiating the surface of the high-dielectric constant insulating film with the plasma to thereby form an oxide film 3 at the interface between the high-dielectric constant insulating film and the substrate (page 4, paragraph 46; see fig. 1C), but Koyanagi fails to disclose expressly wherein the oxide film has a thickness of 6-12 Å.

Referring to figures 1-2B and related text, Buchanan discloses wherein after an oxynitride film 22 is formed, an oxide spacer layer 32 is formed between the oxynitride film and a silicon substrate 12 by a plasma CVD process (col. 6, lines 15-38; see fig. 2B). And the oxide spacer has a thickness between about 1 Å and about 40 Å (col. 4, lines 5-8).

The motivation statement stated in claim 1 also applies.

5. Koyanagi in view of Buchanan discloses [Re claim 46] substantially the claimed limitations, as shown in claim 16. Also, Buchanan discloses wherein forming a gate electrode 14 on the high-dielectric constant gate insulating film (col. 5, lines 65-67; see fig. 1).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a gate electrode on a dielectric layer, as taught by Buchanan, because it would have been to obtain a transistor for an electronic device.

6. Koyanagi discloses [Re claims 18 and 53] wherein the high-dielectric constant insulating film comprises at least one material selected from the group consisting of Al_2O_3, ZrO_2, HfO_2, Ta_2O_5, ZrSiO, HfSiO and ZrAlO (page 4, paragraph 45).

7. [Re claim 20] Koyanagi fails to disclose expressly wherein the oxygen atom-containing gas is O_2 gas.

Buchanan discloses O_2 gas as an oxidizing agent (col. 6, lines 28-35).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use O_2 gas as an oxygen atom-containing gas, as taught by Buchanan, because it would have been to obtain better and high quality oxide film in a plasma process.

8. Claims 8, 11-12, 17, 19 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyanagi in view of Buchanan, as applied to claims 1, 16 and 46 above, and further in view of Suzuki et al. (US Pat. 6497783; hereinafter “Suzuki”).

9. The combined teaching of Koyanagi and Buchanan discloses [Re claim 8] substantially the claimed limitations, as shown in claim 1, but the combined teaching of Koyanagi and Buchanan fails to disclose expressly wherein converting the oxygen atom-containing gas to thereby generate oxygen radicals, and irradiating with the oxygen radicals.

Suzuki discloses radicals of the plasma from processing gas, which are used to process a wafer (col. 29, lines 40-45).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use oxygen radicals of the plasma, as taught by Suzuki, because it would have been to obtain better oxidation at low temperature, and to form an uniform oxide layer.

10. [Re claims 11 and 19] The combined teaching of Koyanagi and Buchanan fails to disclose expressly wherein the process gas comprises at least one rare gas selected from the group consisting of Kr, Ar, He and Xe.

Suzuki discloses an additional or carrier gas of Kr, Ar, He, Xe, and etc. (col. 14, lines 30-60).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a rare gas in a plasma process, as taught by Suzuki, because it would have been to control source gas flow rate and oxidation amount without any unwanted reaction.

11. [Re claim 12] Koyanagi fails to disclose expressly wherein the oxygen atom-containing gas is O_2 gas.

Buchanan discloses O_2 gas as an oxidizing agent (col. 6, lines 28-35).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use O_2 gas as an oxygen atom-containing gas, as taught by Buchanan, because it would have been to obtain better and high quality oxide film in a plasma process.

12. [Re claims 17 and 47] The combined teaching of Koyanagi and Buchanan fails to disclose expressly wherein the plasma is generated based on microwave via a plane antenna member (RLSA) having a plurality of slots.

Suzuki discloses a planar multi-slot antenna for microwave supply (col. 21, lines 54-60).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a planar antenna for plasma process, as taught by Suzuki, because it would have been to obtain plasma with microwaves radiation of a uniform intensity (Suzuki, col. 21, lines 61-67).

13. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching of Koyanagi, Buchanan and Suzuki, as applied to claim 8 above, and further in view of Deboer et al. (US Pub. 2001/0036752; hereinafter “Deboer”).

14. [Re claim 13] The combined teaching of Koyanagi, Buchanan and Suzuki fails to disclose expressly wherein further comprising annealing the substrate after the formation of the oxide film.

Deboer discloses a post-deposition anneals after formation of a dielectric film using O_2 as a source gas (page 2, paragraph 21). Deboer also discloses [Re claim 14] wherein the post-deposition anneal is performed in an oxygen ambient (page 2, paragraph 21), and the oxygen source can be provided using O_2 (page 4, paragraph 34).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to perform a post-deposition anneal, as taught by Deboer, because it would have been to eliminate oxygen vacancies reducing leakage current (Deboer, page 2, paragraph 21).

15. [Re claim 15] Koyanagi fails to disclose expressly wherein the annealing is conducted at a temperature of 500-1100^{o}C.

Referring to figures 1-2B and related text, Buchanan discloses wherein an annealing temperature ranges from 500^{o}C to 1200^{o}C (col. 6, lines 28-30).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to perform annealing process with a certain temperature, as taught by Buchanan, because it would have been to obtain a desired oxide film without any oxygen vacancies or defects.

16. Claims 21-23 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyanagi in view of Buchanan, as applied to claims 16 and 46 above, and further in view of Deboer.

17. [Re claims 21 and 51] The combined teaching of Koyanagi and Buchanan fails to disclose expressly wherein further comprising annealing the surface of the high-dielectric constant gate insulating film and the substrate after the formation of the oxide film.

Deboer discloses a post-deposition anneals after formation of a dielectric film using O_2 as a source gas (page 2, paragraph 21). Deboer also discloses [Re claim 22]

wherein the post-deposition anneal is performed in an oxygen ambient (page 2, paragraph 21), and the oxygen source can be provided using O_2 (page 4, paragraph 34).

The motivation statement stated in claim 13 also applies.

18. [Re claim 23] Koyanagi fails to disclose expressly wherein the annealing is conducted at a temperature of 500-1100^{o}C.

Referring to figures 1-2B and related text, Buchanan discloses wherein an annealing temperature ranges from 500^{o}C to 1200^{o}C (col. 6, lines 28-30).

The motivation statement stated in claim 15 also applies.

19. Claims 29 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyanagi in view of Buchanan, and further in view of Ota (US Pat. 6436777).

20. The combined teaching of Koyanagi and Buchanan discloses [Re claim 29] substantially the claimed limitations, as shown in claim 16. However, the combined teaching of Koyanagi and Buchanan fails to disclose expressly wherein the high dielectric film is a HfSiO film.

Ota discloses a $HfSiO_2$ film as a high dielectric constant material film (col. 8, line 55-col. 9, line 5).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a HfSiO film, instead of using a HfO_2 film disclosed in Koyanagi, because it would have been to obtain less reactive film than HfO_2 film at the interface with a gate electrode (Ota, col. 8, lines 25-30).

The motivation statement stated in claim 16 also applies.

21. The combined teaching of Koyanagi, Buchanan and Ota discloses [Re claim 42] substantially the claimed limitations, as shown in claim 29. And Koyanagi further discloses wherein nitriding the surface of HfSiO film (page 5, paragraph 59).

The motivation statements stated in claims 16 and 29 also apply.

22. Claims 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching of Koyanagi, Buchanan and Ota, as applied to claim 29 above, and further in view of Suzuki.

23. [Re claim 30] The combined teaching of Koyanagi, Buchanan and Ota fails to disclose expressly wherein the plasma is plasma based on microwave via a plane antenna member (RLSA) having a plurality of slots.

Suzuki discloses a planar multi-slot antenna for microwave supply (col. 21, lines 54-60).

The motivation statement stated in claim 17 also applies.

24. The combined teaching of Koyanagi, Buchanan and Ota discloses [Re claim 31] substantially the claimed limitations, as shown in claims 12 and 20, but the combined teaching of Koyanagi, Buchanan and Ota fails to disclose expressly wherein the process gas comprises at least one rare gas selected from the group consisting of Kr, Ar, He and Xe.

Suzuki discloses an additional or carrier gas of Kr, Ar, He, Xe, and etc. (col. 14, lines 30-60).

The motivation statement stated in claims 11 and 19 also applies.

25. Claims 32-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching of Koyanagi, Buchanan and Ota, as applied to claim 29 above, and further in view of Deboer.

26. [Re claim 32] The combined teaching of Koyanagi, Buchanan and Ota fails to disclose expressly wherein further comprising annealing the substrate after the formation of the oxide film.

Deboer discloses a post-deposition anneals after formation of a dielectric film using O_2 as a source gas (page 2, paragraph 21). Deboer also discloses [Re claim 33] wherein the post-deposition anneal is performed in an oxygen ambient (page 2, paragraph 21), and the oxygen source can be provided using O_2 (page 4, paragraph 34).

The motivation statement stated in claim 13 also applies.

27. [Re claims 34 and 35] Koyanagi fails to disclose expressly [Re claim 34] wherein the annealing is conducted at a temperature of 600-1100^{o}C; and [Re claim 35] wherein the substrate is at a temperature from room temperature to 500^{o}C.

Referring to figures 1-2B and related text, Buchanan discloses wherein an annealing temperature ranges from 500^{o}C to 1200^{o}C (col. 6, lines 28-30). The substrate, before annealing process, should be at a temperature below 500^{o}C.

The motivation statement stated in claim 15 also applies.

28. [Re claim 36] Koyanagi fails to disclose expressly wherein the oxide film is formed at a pressure of 3-500 Pa.

Referring to figures 1-2B and related text, Buchanan discloses wherein an oxidizing atmosphere is provided at a pressure between about 1 mTorr and about 20 atm (col. 6, lines 39-43).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a certain pressure for an oxidizing process, as taught by Buchanan, because it would have been to control growth rate of an oxide layer obtaining a desired thickness of the oxide layer.

29. Claims 41 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching of Koyanagi, Buchanan and Ota, as applied to claims 29 and 42 above, and further in view of Bloom et al. (US Pat. 6228779; hereinafter "Bloom").

30. [Re claims 41 and 44] The combined teaching of Koyanagi, Buchanan and Ota fails to disclose expressly wherein further comprising washing the substrate before the formation of the HfSiO film.

Referring to figures 1-2 and related text, Bloom discloses an initial cleaning process of a silicon substrate before growing any films (col. 3, lines 5-12; see step 40).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to clean a substrate before depositing or growing any films, as taught by

Bloom, because it would have been to eliminate any impurities and native oxide layer, which degrade a device performance, before forming an insulating film.

Allowable Subject Matter

31. Claims 28, 39-40, 43, 50, 54 and 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

The statement of reasons for the indication of allowable subject matter was given in the Office Action mailed on August 18, 2008.

Response to Argument

32. Applicants' arguments with regard to the rejections under 35 U.S.C. 103(a) have been fully considered, but they are not deemed to be persuasive for at least the following reasons.

33. Applicants argue that Buchanan does not disclose or suggest a method for forming an underlying film by irradiating the surface of an insulating film disposed on an electronic device substrate with plasma. And applicants also argue that forming an underlying film with a thickness of 6-12 Å by the thermal annealing method disclosed by Buchanan can be very difficult because the re-oxidizing is performed at a relatively high temperature, i.e., between about 500°C and about 1200°C.

First, note that applicants' argument is largely directed to what the cited reference teaches individually. However, it is axiomatic that one cannot show

nonobviousness by attacking references individually where the rejection, as here, is based on a combination of references. *In re Young*, 403 F.2d 754, 159 USPQ 725 (CCPA 1968); *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). For example, applicants argue that Buchanan does not disclose a plasma treatment. However, Koyanagi, not Buchanan, is employed in the rejection to show that feature of the claimed process.

Second, the primary reference, Koyanagi, discloses wherein a heat treatment to form an underlying silicon oxide film 3 may be various methods, including plasma and thermal anneal processes (Koyanagi, page 4, paragraph 46). And Buchanan also discloses wherein an oxynitiride film 22 may be formed by various methods, such as standard thermal treatment or plasma CVD (Buchanan, col. 6, lines 5-25). Therefore, it would have been obvious that a plasma treatment can be used, instead of a thermal annealing process, to form an underlying oxide layer. Both plasma and thermal annealing processes are interchangeable.

Third, Buchanan discloses wherein an underlying oxide spacer layer may have a thickness between about 1 Å and about 40 Å (Buchanan, col. 4, lines 5-9) with a thermal process at a temperature between about 500^{o}C and about 1200^{o}C. Since Buchanan discloses the thickness range, which is very difficult to get using with high temperature range, it would have been obvious to get the thickness range more easily using the plasma treatment discloses in Koyanagi.

Therefore, the claimed limitations are met.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHEUNG LEE whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cheung Lee/
Examiner, Art Unit 2812
March 26, 2009

/Alexander G. Ghyka/
Primary Examiner, Art Unit 2812